CLAIMS

What is claimed is:

1. A flash memory cell comprising:

a substrate of semiconductor material;

a gate structure disposed over the substrate, the gate structure including a first floating gate having a sharp corner; and

a first cap of dielectric material covering the first floating gate, the first cap having one of a substantially square and substantially rectangular cross sectional shape.

2. The flash memory cell according to claim 1, wherein the sharp corner is upwardly flared.

3. The flash memory cell according to claim 1, further comprising a first dielectric Vss spacer covering a generally planar side wall defined by the first floating gate and the first cap.

4. The flash memory cell according to claim 1, wherein the substrate includes a source region, the first floating gate electrically associated with the source region.

5. The flash memory cell according to claim 4, wherein the gate structure further includes a first wordline spacer dielectrically isolated from the first floating gate.

6. The flash memory cell according to claim 5, wherein the substrate further includes a first drain region, the first wordline spacer electrically associated with the first drain region.

7. The flash memory cell according to claim 1, wherein the gate structure further includes a first wordline spacer electrically associated with the first floating gate.

8. The flash memory cell according to claim 7, wherein the substrate further includes a first drain region, the first wordline spacer electrically associated with the first drain region.

9. The flash memory cell according to claim 1, wherein the gate structure comprises a split gate including a second floating gate with a sharp corner.

10. The flash memory cell according to claim 9, wherein the sharp corner of the second floating gate is upwardly flared.

11. The flash memory cell according to claim 9, wherein the second floating gate is covered with a second cap of dielectric material, the second cap having one of a substantially square and substantially rectangular cross sectional shape.

12. The flash memory cell according to claim 11, further comprising a second dielectric Vss spacer covering a generally planar side wall defined by the second floating gate and the second cap.

13. The flash memory cell according to claim 9, wherein the second floating gate is electrically associated with the source region.

14. The flash memory cell according to claim 13, wherein the gate structure further includes a second wordline spacer electrically associated with the second floating gate.

15. The flash memory cell according to claim 14, wherein the substrate further includes a second drain region, the second wordline spacer electrically associated with the second drain region.

16. The flash memory cell according to claim 9, wherein the gate structure further includes a second wordline spacer electrically associated with the second floating gate.

17. The flash memory cell according to claim 16, wherein the substrate further includes a second drain region, the second wordline spacer electrically associated with the second drain region.

18. A method of making a flash memory cell comprising a floating gate with corners each having a sharp, upwardly flared shape, the method comprising the steps of:

providing a substrate of semiconductor material;

forming a mask film over the substrate;

defining a trench in the mask film;

at least partially filling the trench with a first film of electroconductive material; and

etching back a portion of the first film of electroconductive material to partially form the floating gate with the sharp, upwardly flared corners.

19. The method according to claim 18, further comprising the steps of:

at least partially filling the trench with a second film of the electroconductive material;

etching back at least a portion of the second film electroconductive material to increase the sharp, upwardly flared shape of the corners.

20. The method according to claim 19, wherein the etching back step performed after the step of at least filling the trench with the second film of

electroconductive material etches back another portion of the first film of the electroconductive material.

21. The method according to claim 20, further comprising the step of at least partially filling the trench with a dielectric material to form a protective cap over the floating gate.

22. The method according to claim 19, further comprising the step of at least partially filling the trench with a dielectric material to form a protective cap over the floating gate.

23. The method according to claim 18, further comprising the step of at least partially filling the trench with a dielectric material to form a protective cap over the floating gate.

24. The method according to claim 18, wherein the substrate includes at least two shallow trench electrical isolation regions and further comprising the step of removing selected additional portions of the first film of the electroconductive material covering the shallow trench electrical isolation regions to electrically isolate the cell.

25. The method according to claim 19, wherein the substrate includes at least two shallow trench electrical isolation regions and further comprising the step of

removing selected additional portions of the first film of the electroconductive material covering the shallow trench electrical isolation regions to electrically isolate the cell.

26. The method according to claim 20, wherein the substrate includes at least two shallow trench electrical isolation regions and further comprising the step of removing selected additional portions of the first film of the electroconductive material covering the shallow trench electrical isolation regions to electrically isolate the cell.

27. The method according to claim 21, further comprising the step of forming a dielectric Vss spacer along a side wall defined by the floating gate and the protective cap.

28. The method according to claim 22, further comprising the step of forming a dielectric Vss spacer along a side wall defined by the floating gate and the protective cap.

29. The method according to claim 23, further comprising the step of forming a dielectric Vss spacer along a side wall defined by the floating gate and the protective cap.